

Low Loss Air-Gap Spiral Inductors for MMICs Using Glass Microbump Bonding Technique

Jeff Chuang, Samir El-Ghazaly, *Nada El-Zein, *Vijay Nair, *George Maracas, *Herb Gronkin

Department of Electrical Engineering, Center for Solid State Electronic Research,
Arizona State University, Tempe, AZ 85287-5706

*Motorola Inc. Phoenix Corp. Research Labs, 2100 E Elliot Rd., Tempe, AZ 85284

Abstract:

Air-gap spiral inductor structures have been fabricated and integrated with semiconductor substrates using glass microbump bonding (GMBB) techniques. Spiral inductors using air-gap structures have the advantages of low losses, and low parasitic capacitance compared to conventional inductors on doped silicon semiconductor substrate. Stacked air-gap spiral inductors on GaAs substrates using GMBB techniques also can reduce the inductor area. Because the glass microbump bonding techniques are simple, this bonding technique provides an alternative integration approach for monolithic microwave integrated circuits (MMICs). Experimental results of air-gap spiral inductor on both silicon and GaAs substrates are presented in this paper.

INTRODUCTION

The development of new generation digital wireless communication systems is constrained by cost, size, and power considerations [1]. This resulted in rapid growth in monolithic microwave integrated circuits (MMICs) research to meet the increased performance demands. The spiral inductor is one of the main components in MMIC's. To meet circuit level performance demands, several factors must be considered for inductor design including high quality-factors (Q), high resonant frequency (f_R) and adequate inductance (L) using a small area. The integration of inductors on both silicon and GaAs substrates presents several difficult tasks using standard semiconductor processing. The main concern about the inductor fabricated on low-cost silicon is the high substrate dielectric losses due to low substrate resistivity. On the other hand, the reduction of chips area is crucial for the economic production of GaAs integrated circuits. The stacked

spiral inductor structures proposed in 1985 has shown some potential for MMICs [2]. This double-layered inductor structures can enhance magnetic flux of the inductor due to additional upper metal coil, therefore a given inductance can be achieved at minimum metal wire routing which can reduce both inductor resistance, to improve its Q factor, and inductor area, to reduce chip size. Recent successful demonstrations of multilevel-spiral (MLS) inductor structure [3] for silicon technology and air-gap stacked inductor structures [4] on GaAs substrates show continuous improvements in stacked spiral inductor design. However, the high dielectric constant inter-metal material in MLS inductor structures has lowered its resonant frequency. In addition, the air-gap stacked inductor fabricated using the air-bridge process limits the air-gap height top about 3- 4 μm .

In this paper, we present air-gap spiral inductor structures using glass microbump bonding (GMBB) technique [5]. The main idea of this approach is that low loss glass substrates with precise controlled glass bump height can be used as the upper metal layer support. The air-gap height of the spiral inductor using this bonding method can be controlled as high as 30 μm , therefore the parasitic capacitance can be minimized to enhance the resonance frequency. The performance of different inductive structures will be examined for structure optimizations

DESIGN AND FABRICATION

There are mainly two types of losses in a transmission line: a dielectric substrate loss and the conductor loss. Because our GMBB inductor structures design has transmission propagated along the glass for upper metal coil, any additional losses

due to glass substrate will degrade the device performance. In order to verify the losses in glass substrate, coplanar waveguide (CPW) structure was first fabricated on glass, semi-insulating GaAs, 4000 $\Omega\text{-cm}$ high resistivity (HR) silicon, and 30 $\Omega\text{-cm}$ resistivity silicon substrates for losses analysis. In this analysis, only the doped silicon substrate was deposited with 2 μm of SiO_2 layer for DC blocking. Fig. 1 shows the attenuation of 1.5 μm -thick gold metal transmission line on various substrates. The loss analysis results confirm that glass substrate has the lowest losses ($\sim 0.12\text{dB/cm}$ at 3 GHz) comparing to other substrates. This small amount of losses mainly come from conductor loss and radiation loss of the CPW configuration.

We studied two different configurations of inductors of the same rectangular inductor area (700 μm X 720 μm) with different inductor inner loop area. Fig. 2 (a) is the photograph of the inductor with larger inner coil area (280 μm X 300 μm) with the line/space = 20 μm / 20 μm (LA). Fig. 2 (b) is the inductor with smaller inner coil area (220 μm X 200 μm) with the line/space = 20 μm / 30 μm (SA). There are three types of inductors structures (as shown in Fig.3) designed using these two different configurations. Fig. 3 (a) is the top view of the conventional spiral inductor. Fig. 3(b) is the air-gap spiral inductor with the inductor coil fabricated on glass substrate and semiconductor surface as ground plane. Fig. 3(c) is the stacked air-gap spiral inductor.

For both the conventional and stacked air-gap spiral inductor, the ground plane was placed 140 μm apart from both side edges of inductor as coplanar waveguide structures. All inductors structures were designed to include a 420 μm long CPW microwave launcher for on-wafer characterization. The fabrication process of glass microbump can be found in [5]. To further investigate the relation between air-gap height and parasitic capacitance of inductors, several different turns of air-gap spiral inductors with different glass bump height were fabricated. The thickness of both GaAs and silicon substrates was about 550 μm . The gold metal thickness for the inductor coil was 1.5 μm .

RESULT AND DISCUSSION

S-parameter of spiral inductors were measured using HP8510 network analyzer with a Short-Open-Load one port calibration routine. Table I shows the inductance (L) and resonance frequency (fr) of different types of inductors. The air-gap height for both air-gap and stacked spiral inductor was 15 μm . The comparison between larger inner loop inductor (LA1) and smaller inner loop inductor (SA1) showed that even both LA and SA have same inductor area, LA configuration will have larger inductance value compared to SA inductor. This is because that the self-inductance of an inductor depends strongly on the inner loop area. Furthermore, the smaller line-to-line distance in LA configuration can further enhance the mutual inductance of the inductor by reducing flux leakage. However, inductor in LA configuration has smaller resonant frequency comparing to that of SA configuration. This is mainly due to the reduced lines spacing in LA configuration which increases the parasitic capacitance of inductor.

The measurement results showed that air-gap spiral inductors have smaller inductance value compared to that of conventional spiral inductor. The reason for this is that air-gap spiral inductors have shorter metal length in our inductor design. The air-gap transmission structures using glass substrate have very small effective dielectric constant compared to that of conventional inductors have metal lines laid on high dielectric semiconductor substrates. Thus, air-gap inductors will have parasitic capacitance smaller than conventional inductors, as indicated in Table I. Hence, air-gap spiral inductors have higher resonant frequency.

Ideally, the inductance value of stacked inductors can be increased up to 3-4 times of that of nonstacked inductors. The inductance value of our stacked inductors is about twice the value of nonstacked structures. This can be due to using offset stacked spiral inductive structures [2], and large air-gap distance between lower and upper coils, hence the magnetic flux was not optimized in our stacked inductors. However, the resonant frequency of stacked inductors only decreased by about 15% compared to conventional inductors, which demonstrated the merits of low parasitic capacitance of air-gap structures. Fig. 4 shows the parasitic capacitance of air-gap inductors as a

function of glass bump height. The results show that capacitance value of the inductors follow the relation of $C \sim \epsilon_r/d$, where ϵ_r is effective dielectric constant and d is the bump height. As the number of turns of the inductors is increased, the air-gap height becomes an important factor in reducing parasitic capacitance.

CONCLUSIONS

The important factors to be considered for the design of inductors have been discussed in this paper. For a given inductor area, the inductance can be enhanced by increasing the inductor inner loop area, reducing the line-to-line spacing, and using stacked inductor structures. In contrast, parasitic capacitance will be increased due to inductance optimization which limits the inductor operation frequency range. Air-gap inductors and air-gap stacked inductors using glass microbump bonding technique are able to maintain the desired inductance value without degrading the inductors operation frequency range. Furthermore, the processing of low loss glass substrates was done separately from standard semiconductor fabrication processes. The bonding can be performed at final stage of circuit packaging. This bonding approach does not require any modification of the standard semiconductor processing. This paper demonstrated

the advantages of air-gap spiral inductor using glass microbump bonding method. The potential of using this bonding method for MMICs applications is encouraged.

REFERENCES

1. L. M. Burns, "Applications GaAs and Silicon Integrated Circuits in Next Generation Wireless Communication Systems," IEEE J. Solid-State Circuit, vol. 30, pp. 1088-1095, Oct. 1995.
2. M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins and R. H. Jansen, "Miniature Mutilayer Spiral Inductors for GaAs MMICs," GaAs IC Symposium, pp. 303-306.
3. J. N. Burghartz, K. A. Jenkins, and M. Soyuer, "Multilevel -Spiral Inductors Using VLSI Interconnect Technology," IEEE Electron Device Lett., vol. 17, pp. 428-430, Sept. 1996.
4. S. W. Paek and K. S. Seo, "Air-Gap Stacked Spiral Inductor," IEEE Microwave and Guided Wave Letters, vol. 7, No. 10, Oct. 1997.
5. J. Chuang, S. El-Ghazaly, D. Schroder, Y. Zhang, G. Maracas, A. Reyes, "Air-Gap Transmission Lines for OEICs and MMICs Using Glass Substrates," IEEE MTT-S Digest, Vol. 1, pp. 256-259, 1997.

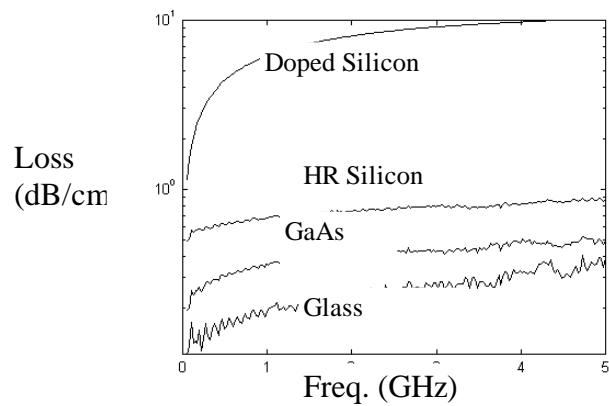


Fig. 1. Measured losses of CPW transmission on different types of substrates.

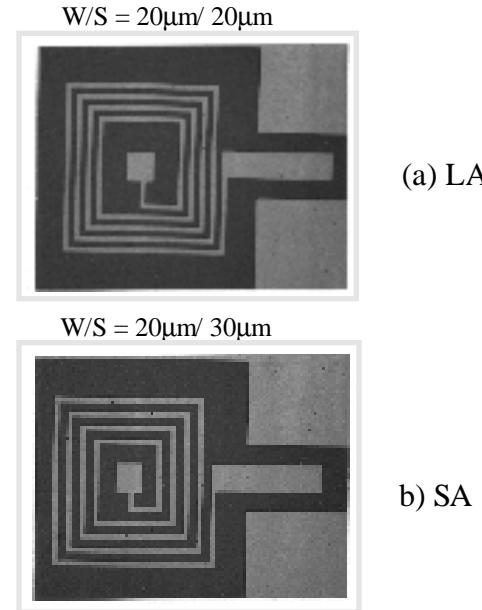


Fig. 2. Photographs of 4-turn spiral inductor of the same inductor area (700μm x 720μm) with different inner loop area. (a) Large inner loop. (b) Small inner loop.

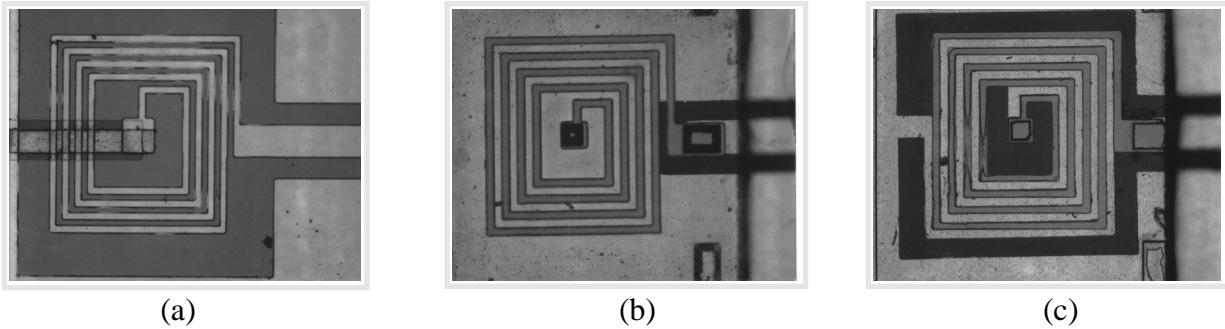


Fig. 3. Photographs of various types of inductors. (a) Conventional inductor. (b) Air-gap inductor. (c) Stacked inductor.

		L (nH)	fr (GHz)
Conventional Inductor	LA1	12	3.1
	SA1	9	3.5
Air-Gap Inductor	LA2	10	4.1
	SA2	8	4.4
Stacked Inductor	LA2	30	2.5
	SA2	25	2.8

Table I : The inductance and resonance frequency of different types of inductors.

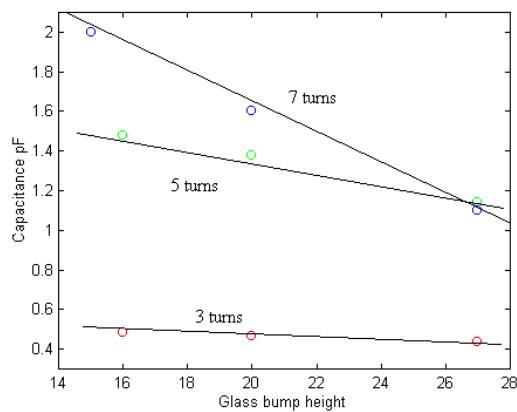


Fig. 4 The parasitic capacitance values for different turns of air-gap inductors with different bump height.